In the Claims

The following listing of claims replaces all prior listings and versions of claims in this application.

1. (Currently amended) A processor comprising:

a plurality of registers;

circuitry configured to process a plurality of instructions associated with an instruction set including a plurality of branch and non-branch instructions, the plurality of instructions each having a multi-byte length, the plurality of instructions accessible at multi-byte aligned addresses;

common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of [[said]] an immediate field in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions; and

wherein ~~substantially all~~ the multi-byte aligned branch instructions are operable to access [[all]] the plurality of instructions at byte aligned addresses, wherein each of the multi-byte aligned branch instructions has a start address that is an integer multiple of a byte aligned address and the integer multiple is greater than one.

2. (Original) The processor of claim 1, wherein the plurality of instructions are accessed at word aligned addresses.

3. (Original) The processor of claim 1, wherein the plurality of instructions are accessed at half-word aligned addresses.

4. (Currently amended) The processor of claim 1, wherein accessing the instructions comprises reading to and writing from the addresses.

5. (Currently amended) The processor of claim 1, wherein the branch instructions comprise branch and conditional branch instructions.

6. (Currently amended) The processor of claim 1, wherein the branch instructions comprise a branch offset and a current program counter value.

7. (Currently amended) The processor of claim [[1]] 6, wherein the units of branch offset and current program counter are in bytes.

8. (Original) The processor of claim 1, wherein the plurality of instructions are one word in length.

9-13. (Canceled)

14. (Currently amended) A field programmable gate array, comprising:

a plurality of registers;

circuitry configured to process a plurality of instructions including a plurality of branch instructions and a plurality of non-branch instructions associated with an instruction set, one of the plurality of branch instructions including an immediate field and one of the plurality of non-branch instructions including an immediate field; and

common subcircuitry that performs a sign extension of [[an]] the immediate field associated with the one ~~or more~~ of the branch instructions and that performs a sign extension of [[said]] the immediate field associated with the one ~~or more~~ of the non-branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions, wherein the sign extension of the immediate field associated with the one ~~or more~~ of the branch instructions is performed to determine a branch target address; [[and]] wherein each of the plurality of branch instructions and non-branch instructions has a multi-byte length, has a start address that is an integer multiple of a byte aligned address, and is operable to access [[all]] the plurality of instructions at byte aligned addresses, wherein the integer multiple is greater than one.

15. (Canceled)

16. (Currently amended) The field programmable gate array of claim [[15]] 14, wherein the plurality of instructions are accessed at half-word aligned addresses.

17. (Previously Presented) The field programmable gate array of claim 14, wherein branch instructions comprise branch and conditional branch instructions.

18. (Currently amended) The field programmable gate array of claim 14, wherein the common subcircuitry is used to handle the immediate field associated with the one of the branch instructions and the immediate field associated with the one of the non-branch instructions and wherein an immediate field value of each of the immediate fields is maintained in units of bytes.

19. (Currently amended) The field programmable gate array of claim 18, wherein common subcircuitry is used to perform sign-extensions of the immediate field associated with the one of the branch instructions and the immediate field associated with the one of the non-branch instructions.

20-30. (Canceled)

31. (Currently amended) The processor of claim 1, wherein one of a primary or secondary component accesses memory of the processor directly through ports without access through a system bus, and wherein the processor is implemented on a field programmable gate array that does not comprises a system bus.

32. (Previously Presented) The field programmable gate array of claim 14, wherein one of a primary or secondary component accesses memory of the field programmable gate array directly through ports without access through a system bus, and wherein the array does not comprises a system bus.